REMARKS

In the Office Action, the examiner rejected Claims 1-19 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-33 of U.S. Patent No. 6,678,645. Accordingly, the applicant has submitted concurrently herewith a terminal disclaimer accompanied by a prescribe fee to overcome the rejection based on the judicially created doctrine of obviousness-type double patenting.

In the Office Action, the examiner rejected Claims 1-19 under 35 U.S.C. 102(b) as being anticipated by Komoto (cited reference, U.S. Patent No. 5,740,086). Accordingly, the applicant has amended the independent claims (Claims 1, 9, 10 and 19) for more clearly differentiate the present invention from the technology disclosed by the cited Komoto reference. The applicant believes that the present invention defined in the claims as amended cannot be anticipated by Komoto as discussed below.

The objective of the present application is to provide an effective method to validate a complex IC, typically, system-on-a-chip (SoC) design by using silicon ICs and an event based test system (event tester). The context apparatus of the present application is the event based test system which has an architecture different from any existing test system.

In semiconductor IC testing, there are primarily two types of tester architecture for testing semiconductor devices. One is a traditional cyclized tester (cycle based test system), which is

used in the industry today, where test data for defining such as waveforms and timings of test patterns are described with respect to predefined time sets and test cycles. Another type of test system architecture is an event tester (event based test system) which is newly proposed by the assignee of the present invention. The feature in the present invention is based on the event based test system which can effectively utilize the data produced through the electronic design automation (EDA) environment.

There are fundamental difference between the cycle based test system and the event based test system. The event based test system is unique in that it incorporates the concept of "event" rather than the traditional "test cycle" and "time sets" for generating the test signals and strobes (test vectors). The event is defined as any changes in a signal generated by the test system for testing the DUT relative to a predetermined reference timing point. The timing of each event is expressed by a difference between two adjacent events. In a traditional cycle based test system, the timing edges of the test signal are defined relative to a test cycle (i.e., a fixed reference rate), such as a starting edge of a respective test cycle by selecting one or more time sets. Because the conventional cycle based test system has to specify each "waveform" and use predefined "time sets" relative to the test cycle for selecting the timing of the waveform, flexibility in generating the test signals and strobes is significantly limited compared to the event based test system.

To clarify the feature of the present invention and to overcome the rejection by the examiner, the applicant has amended Claims 1, 9, 10 and 19 to clarify the meaning of the event timing. Namely, Claims 1, 9, 10 and 19 now include the limitation that the timing of the event represents a time difference between two adjacent events. The cited Komoto reference does not show or suggest any of the features of the event based test system of present invention as discussed in detail below.

The cited Komoto reference discloses a semiconductor test system for testing a semiconductor device by using CAD data produced for the design of the semiconductor device. The test system in the cited Komoto reference patent includes an event memory for storing event data indicating existence of waveform changes in the test vector with respect to the data indicating the terminals, a delay data memory for storing delay time data indicating the time when the waveform change arises as a time difference from the reference period, and a waveform data memory for storing waveform data indicating the waveform change when there is a change in the waveform.

These memories disclosed by the cited Komoto reference appear to correspond to the event memory in the event test system of the present invention. Please note that the structure of the event test system is disclosed by the references incorporated in the instant application. The cited Komoto reference also includes the word "event". However, even though the word "event" is used, the

semiconductor test system of Komoto is a traditional cycle based test system. The event and its waveform in the cited Komoto reference are defined with reference to the reference period as evidenced by the descriptions, for example, at column 5, lines 48-56 with reference to Figure 5, which reads as follows:

> The events occurred in the intermediate of the reference period of 10 nanosecond, such as 15 nanosecond, 26 nanosecond, 37 nanosecond, are expressed by the delay times from the immediately prior reference period and transferred to delay data memory 38. For example, the event of 15 nanosecond is expressed as a 5 nanosecond delay from the 10 nanosecond reference period and such data is transferred to the delay data memory 38.

From the above excerpts, it is clear that the "reference period" is a fixed reference cycle (ex. 10 nanosecond) equivalent to a "test cycle" in the cycle based test system. In other words, the test system in the cited Komoto is a cycle based test system which is so designed that the CAD data in the event format can be directly used therein. To use the event data in the cycle based test system, it is necessary to always specify a timing and waveform of a particular event with reference to the reference period as shown in Figure 5. In other words, the cited Komoto reference does not show or suggest the idea of utilizing the event based test vectors by the event based test system.

Therefore, the concept as well as the apparatus of the present application is fundamentally different from the context and apparatus disclosed by the cited Komoto reference. The use of event based test system is essential for implementing the method of the present invention. All of the independent claims (Claims 1, 9,

10 and 19) in the present application identify this requirement explicitly.

As noted above, significant differences exist between the present invention and the semiconductor test system disclosed by the cited Komoto reference. Therefore, the applicant believes that the present invention is not anticipated by Komoto.

In view of the foregoing, the Applicant believes that Claims 1-19 are in condition for allowance, and accordingly, the applicant respectfully requests that the present application be allowed and passed to issue.

Respectfully submitted,

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